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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/600,186	06/20/2003	Masud Beroz	TESSERA 3.0-297	8841
530	7590	03/08/2006	EXAMINER IM, JUNGHWA M	
LERNER, DAVID, LITTENBERG, KRUMHOLZ & MENTLIK 600 SOUTH AVENUE WEST WESTFIELD, NJ 07090			ART UNIT 2811	PAPER NUMBER

DATE MAILED: 03/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/600,186	BEROZ, MASUD	
	Examiner	Art Unit	
	Junghwa M. Im	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 19 December 2005.
- 2a) ☒ This action is FINAL. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-19 is/are pending in the application.
- 4a) Of the above claim(s) 16-19 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-15 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

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DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-2 and 4 are rejected under 35 U.S.C. 102(b) as being anticipated by Dishongh et al. (US 6452502), hereinafter Dishongh.

Regarding claim 1, Fig. 1 of Dishongh shows a semiconductor chip [100] having a body [102] with oppositely directed front and rear surfaces, contacts on said front surface and internal components [112, 114] within said body electrically connected to said contacts on said front surface, said chip also having pads [108] on said rear surface electrically isolated from said internal components and traces [110] on said rear surface electrically connected to said pads.

Regarding claim 2, Fig. 1 of Dishongh shows internal components include active devices [114].

Regarding claim 4, it is inherent that the back of the semiconductor device said body has edges bounding said front and rear surfaces and said traces include bonding points disposed in the vicinity of said edges.

Claim Rejections - 35 USC § 103

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The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dishongh in view of Wenzel (US 6150714).

Regarding claim 3, Fig. 1 of Dishongh shows substantially the entire claimed structure except "said internal components consist only of passive devices." Wenzel discloses the internal components consist only of passive devices [col. 18, lines 49-50].

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Wenzel into the device of Dishongh in order to have the internal components consisting only of passive devices to accommodate the required circuit specification.

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wenzel in view of Dishongh.

Regarding claim 5, Fig. 8 of Wenzel shows a chip assembly comprising;

(a) a first semiconductor chip [104] including a first body [104a, 104b] with oppositely-directed front and rear surfaces, said first semiconductor chip having internal components within said first body, contacts on the front surface connected to said internal components, said first semiconductor chip also having pads [312 in Fig. 14] on the rear surface

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of said first body and traces [310 in Fig. 14] extending from said pads along the rear surface of the first body;

(b) a second semiconductor chip [102] including a second body [102a, 102b] with oppositely-directed front and rear surfaces, said second semiconductor chip having internal components within the second body and contacts on the front surface of the second semiconductor chip,

said second semiconductor chip being mounted on said first semiconductor chip so that said second semiconductor chip overlies said rear surface of said first semiconductor chip, said contacts of said second semiconductor chip being electrically connected to said pads of said first semiconductor chip.

Wenzel fails to show that “said chip also having pads on said rear surface electrically isolated from said internal components and traces on said rear surface electrically connected to said pads.” Fig. 1 of Dishongh shows that a chip having pads [108] on the rear surface electrically isolated from the internal components and traces [110] on said rear surface electrically connected to the pads.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Dishongh into the device of Wenzel in order to have the pads of each chip on the rear surface electrically isolated from the internal components and traces on said rear surface electrically connected to said pads for a additional signal routing.

Claims 6-13 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wenzel and Dishongh as applied to claim 5 above, and further in view of Akram et al. (US 6313522), hereinafter Akram.

Regarding claim 6, the combined teachings of Wenzel and Dishongh show the most aspect of the instant invention except “said front surface of said second semiconductor chip confronts said rear surface of said first semiconductor chip.” Fig. 5 of Akram shows a configuration of the stacked chips wherein said front surface [22A] of said second semiconductor chip [22] confronts said rear surface [20B] of said first semiconductor chip [20].

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Akram into the device of Wenzel and Dishongh in order to have said front surface of said second semiconductor chip confronted said rear surface of said first semiconductor chip to accommodate the design specification.

Regarding claim 7, Fig. 2 of Akram shows said contacts of said second semiconductor chip are bonded to said pads of said first semiconductor chip by masses of electrically conductive bonding material.

Regarding claim 8, Fig. 5 of Akram shows a substrate [12], said chips being mounted on said substrate with said front surface of said first semiconductor chip facing toward said substrate, said contacts of said first semiconductor chip being electrically connected to said substrate, said traces of said first semiconductor chip also being electrically connected to said substrate so that said contacts of said second semiconductor chip are connected to said substrate through said pads and traces of said first semiconductor chip [through metal layers 114, 116, 120].

Regarding claim 9, Fig. 2 of Akram shows bonding wires extending between said traces and said substrate, said traces being electrically connected to said substrate [12] through said bonding wires.

Regarding claim 10, Fig. 1 of Dishongh shows said first semiconductor chip has edges bounding said front and rear surfaces of said first body, and wherein said bonding wires are connected to said traces adjacent said edges.

Regarding claim 11, Fig. 2 of Akram shows said contacts of said first semiconductor chip are connected to said substrate by masses of bonding material disposed between said contacts of said first semiconductor chip and said substrate.

Regarding claim 12, Akram discloses said contacts of said first semiconductor chip are connected said substrate by leads extending between said contacts of said first semiconductor chip and said substrate [col. 1, line 42-45].

Regarding claim 13, Fig. 8 of Wenzel shows said substrate is a package substrate adapted for mounting on a circuit panel.

Regarding claim 15, Fig. 2 of Akram shows said second semiconductor chip has pads and traces on the rear surface of said second body, the traces of said second semiconductor chip being electrically connected to said substrate, the assembly further comprising a third semiconductor chip [24] overlying said rear surface [22B] of said second semiconductor chip [22] and electrically connected to said pads of said second semiconductor chip.

Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wenzel, Dishongh and Akram as applied to claim 13 above, and further in view of Distefano (US 6309915).

Regarding claim 14, the combined teachings of Wenzel, Dishongh and Akram show the substantially the entire claimed structure except “wherein said substrate has terminals adapted for connection to a circuit panel, said terminals being movable with respect to said first semiconductor chip.” Distefano discloses a movable terminal movable with respect to the chip [col. 4, lines 11-18].

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Akram, Dishongh and Akram into the device of Wenzel in order to have the substrate with terminals adapted for connection to a circuit panel, said terminals being movable with respect to said first semiconductor chip to facilitate testing and assembly.

Response to Arguments

Applicant's arguments filed December 19, 2005 have been fully considered but they are not persuasive.

Applicant mainly argues that “Dishongh discloses two separate chips with connections on only one side of each chip. Neither the integrated circuit package 102 nor the printed circuit board 104 have contacts on a front surface and pads on a rear surface as specifically recited in claim 1. Thus, Dishongh does not disclose or suggest all of the elements of claim 1.” Examiner disagrees. Fig. 1 of Dishongh explicitly shows contacts on the front of the IC package. For

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example, it is well known in the art that a symbol 'T' connected at the end of the resistor designates a power supply. And one of ordinary skill in the art readily understands that the power is fed through the front surface, thus requiring a contact on the first surface, especially in this configuration since the rear surface is connected to conductive traces of the circuit board. Also note that an element 102 is an integrated circuit within the body of the IC package (col. 3, lines 33-35), further indicating that there are many other internal components which require signal feeding through the front surface. This aspect is shown in Fig. 2. Therefore, Dishongh discloses all of the elements recited in claim 1. Applicant presents an argument as if having contacts/pads on the surface of the chip carries patentable distinction, however, Examiner would like to point out that contacts/pads are merely a portion/region/area on the front/rear surface of the chip to make a connection to a signal. One of ordinary skill in the art understands that contacts/pads are frequently omitted in an artist's rendition.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

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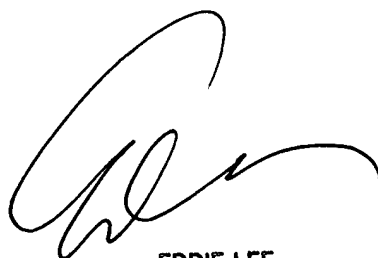
however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Junghwa M. Im whose telephone number is (571) 272-1655. The examiner can normally be reached on MON.-FRI. 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's acting supervisor, Eddie C. Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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